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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/389,491	09/03/1999	KI-YOUNG LEE	028213-0101	5458

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LEE & STERBA, P.C.
1101 WILSON BOULEVARD
SUITE 2000
ARLINGTON, VA 22209

EXAMINER	
BROCK II, PAUL E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 02/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/389,491	LEE ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12,14-24 and 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12,14-24 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 1999* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 12, 14 – 16, 18 – 22, 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gambino et al. (USPAT 6166423, Gambino) in view of Kuwajima (USPAT 5534461).

Gambino discloses a method of making a semiconductor integrated circuit capacitor in figures 11 – 26.

With regard to claim 12, Gambino discloses in figure 11 providing an insulating substrate (305). Gambino discloses in figure 11 simultaneously forming a first wire line (315) and a lower electrode (310) on predetermined surfaces of the insulating surfaces. Gambino discloses in figure 11 forming an interlevel insulating layer (307) on the substrate, on the first wire line, and on the lower electrode. Gambino discloses in figure 12 selectively etching the interlevel insulating layer to expose a predetermined surface of the lower electrode and a predetermined surface of the first wire line thereby simultaneously forming in the interlevel insulating layer: (i) a first via hole (320) having sidewalls and disposed above the lower electrode; and (ii) a second via hole (330) disposed above the first wire line. Gambino discloses in figure 13 forming a

tungsten containing conductive layer (328) on the interlevel insulating layer and in the first and second via holes, including on the exposed predetermined surfaces of the lower electrode and first wire line. Gambino discloses in figure 14 performing a tungsten etch back process to selectively etch back the tungsten containing conductive layer on the interlevel insulating layer and in the first and second via holes to form: ii) a tungsten containing conductive plug from the tungsten containing conductive layer formed in the second via hole on the predetermined surface of the first wire line from the tungsten containing conductive layer formed in the second via hole, and iii) an exposed surface containing the conductive plug, the predetermined surface of the lower electrode, and predetermined surfaces of the interlevel insulating layer. Gambino does not disclose etching back the conductive layer to form a spacer on the sidewalls of the first via hole. Kuwajima teaches in figures 1 – 4, 10 and 18, the abstract and column 7, lines 50 – 62 performing a tungsten etch back process to selectively etch back a tungsten containing conductive layer (14) on an interlevel insulating layer (12) and in the first and second via holes (15c and 15b, respectively) to form: i) a tungsten containing conductive sidewall spacer on sidewalls of the first via hole and a portion of an exposed predetermined surface of a lower electrode (13b left of center in via 15c) from the tungsten containing conductive layer formed in the first via hole for preventing dielectric disconnection; ii) a tungsten containing conductive plug in the second via hole on the predetermined surface of a first wire line (13b above right most region 8) from the tungsten containing conductive layer formed in the second via hole, the tungsten containing conductive sidewall spacer and the tungsten containing conductive plug being formed of the same tungsten containing conductive layer; and iii) an exposed surface containing the spacer, conductive plug, a portion of the predetermined surface of the lower

electrode not covered by the tungsten containing conductive sidewall spacer, and predetermined surfaces of the interlevel insulating layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the tungsten etch back process of Kuwajima in the method of Gambino in order to form wiring layers having a good buring state, a good coverage state and a planarized surface to maintain good step coverage as stated by Kuwajima in the abstract and column 1, lines 13 – 15. Gambino discloses in figure 15 forming a dielectric layer (322 on the exposed surface, and the tungsten containing conductive layer formed in the first via hole. It would have been further obvious in the method of Gambino and Kawajima that the dielectric layer would be formed tungsten containing conductive sidewall spacer. Gambino discloses in figure 16 removing the dielectric layer on the exposed surface except for a predetermined portion of the dielectric layer disposed on the first via hole and predetermined surface of the lower electrode. It is further obvious in the method of Gambino and Kawajima that the removing would include removing the dielectric layer on the exposed surface except for a predetermined portion of the dielectric layer disposed on the tungsten containing conductive sidewall spacer. Gambino discloses in figure 18 simultaneously forming: (i) a second wire line (left most 324) connected to the tungsten containing conductive plug; and (ii) an upper electrode connected to the dielectric layer.

With regard to claim 14, Gambino discloses in column 5, line 33 that the dielectric layer has a structure a single-level structure containing an oxide layer.

With regard to claim 15, Gambino discloses in column 8, lines 7 –11 the oxide layer is made using a deposition technique employing Plasma Enhanced Oxide (PEOX). It is inherent that PECVD as described in line 17 is the same as PEOX when depositing oxide.

With regard to claim 16, Gambino discloses in column 6, lines 13 – 17 the nitride layer is made using a deposition technique employing Plasma Enhanced Nitride (PESiN). It is inherent that PECVD as described in line 17 is the same as PESiN when depositing nitride.

With regard to claim 18, Gambino discloses in column 5, lines 31 – 45 the lower and upper electrodes are made of aluminum. It is inherent that aluminum used in the processing of silicon wafers is an alloy of aluminum and silicon.

With regard to claim 19, Gambino discloses in column 5, lines 37 – 39 an anti-reflection layer is disposed on the lower and/or upper electrode's surface.

With regard to claim 20, Gambino discloses I column 5, lines 37 – 39 wherein the anti-reflection layer has a single level structure comprised of Ti.

With regard to claim 21, Gambino discloses in column 5, lines 37 – 39 a barrier layer is disposed on the lower and/or upper electrode's surface.

With regard to claim 22, Gambino discloses in column 5, lines 37 – 39 wherein the barrier layer has a single level structure comprised of Ti.

With regard to claim 24, Gambino discloses in column 7, lines 39 – 48 the interlevel insulating layer is selectively etched by the process of dry etching. Reactive ion etching, as disclosed in column 7, line 48 is a dry etching process.

With regard to claim 26, Kuwajima teaches in figures 1 – 4, 10 and 18, the abstract and column 7, lines 50 – 62 that the spacer formed on the sidewalls of the via hole has a sloping surface.

3. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gambino and Kuwajima as applied to claims 12 and 14 above, and further in view of Oh et al. (USPAT 6074907, Oh).

It is not clear if Gambino and Kuwajima teach that the dielectric layer has a multi-level structure containing layers selected from the group consisting of oxide layers, nitride layers, and mixtures thereof. Oh teaches in column 4, lines 49 – 51 a dielectric layer that has a multi-level structure consisting of oxide/nitride/oxide layer (ONO). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the ONO layer of Oh in the process of Gambino and Kuwajima in order to form a high capacitance capacitor dielectric material.

4. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gambino and Kuwajima as applied to claim 12 above, and further in view of Nulty et al. (USPAT 6066,555, Nulty).

It is not clear if Gambino and Kuwajima teach further comprising, after forming the first and second via holes, RF sputter etching the interlevel insulating layer and the first and second

via holes. Nulty teaches in column 2, lines 56 – 60 RF sputter etching an interlevel insulating layer and via holes. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the RF sputter etching of Nulty in the process of Gambino and Kuwajima in order to remove native oxide on top of the conducting layers as stated by Nulty in column 2, lines 56 – 60.

Response to Arguments

5. Applicant's arguments filed December 12, 2002 have been fully considered but they are not persuasive.

6. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
February 7, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800